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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,643	11/29/2001	Keiji Inoue	36856.585	8176

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,643	INOUE ET AL.	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 10-14* is/are allowed.

6)☒ Claim(s) *5-9 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The request filed on 01/09/04 Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/995,643 is acceptable and a RCE has been established. An action on the RCE follows.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "plurality of module substrates are stacked ***in a direction perpendicular to a surface*** of said motherboard" claim 5, lines 11-12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 5 is objected to because of the following informalities:

Claim 5, line 16, "a surface of said motherboard" should be –the surface of said motherboard—for proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, lines 11-14, it is unclear. The phrase of "said plurality of module substrates...**perpendicular to a surface of said motherboard**...**parallel to the surface of said motherboard**" is not understood. Applicant should clarify this limitation.

Examiner assumes that this limitation should be –said plurality of module substrates are stacked on a surface of said motherboard and are sequentially offset from one to the other in the direction parallel to the surface of said motherboard—for providing proper structure of the claims based on the teaching of the drawings.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 5-6, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (US 5,323,060).

As best understood to claim 5, Fogal et al. disclose a module substrate mounting structure (10), column 2, lines 31-33, as shown in figures 1-3 comprising:

a motherboard (multi-chip substrate 12), column 2, line 34, inherently having connecting pads (not shown) disposed on a surface thereof; and

a plurality of module substrates (18, 28), or (18, 28, and 54), see figure 1, each having connecting members (44; 50; 56), see figure 1, attached to a surface thereof via connecting terminals (26, 36,and 60), column 2, lines 54, 65, and column 3, line 20, disposed on each of said plurality of module substrates (18, 28, and 54); wherein

said module substrates (18, 28, 54) are stacked with a space therebetween on said motherboard (see figures 1), said connecting members (44, 50, and 56) of said module substrates (18, 28, and 54) are electrically connected to the to said connecting pads on said motherboard (12), said connecting terminals are arranged along an edge portion of each of said module substrates,

said module substrates (18, 28, and 54) are stacked on said motherboard and are sequentially offset from one another in the direction parallel to the surface of said motherboard (12), said edge portions with said connecting terminals disposed thereon are aligned with one another in the direction perpendicular to the surface of said motherboard, and said connecting pads (pads on the substrate 12) connected to said connecting terminals (26, 36,and 60) arranged along the edge portion of each of said

substrates via said connecting members (wires 44, 50, 56) **are arranged in the same row.**

Regarding claim 6, Fogal et al. disclose a lower substrate (18-figure 1) recognition mark is located on an exposed portion of a lower module substrates of said plurality of module substrates (18, 28, and 54).

Regarding claim 8, Fogal et al disclose a ratio of a length to a width of each of said module substrates is within a range of about 1/3 to about 1/1, see figure 1.

7. Claims 15, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (5,874,781).

As to claim 15, Fogal et al. disclose a module substrate mounting structure (10), column 3, lines 24-26 as shown in figures 1-3 comprising:

a motherboard (12), column 3, line 26, inherently having connecting pads (not shown) disposed on a surface thereof; and

a plurality of module substrates (18, 28), column 3, lines 39-40, 47, each having connecting members (44, 50), column 4, lines 38, 41, attached to a surface thereof via connecting terminals (bonding pads 26, 36), column 3, lines 45, 50, disposed on each of said plurality of module substrates (18, 28); wherein

said module substrates (18, 28) are stacked with a space therebetween, see figure 1, on said motherboard (12), said connecting members (44, 50) of said plurality of module substrates (18, 28) are electrically connected to the to said connecting pads (not shown) on said motherboard (12), said connecting terminals (pads 26, 36) are

arranged along a pair of edge portions (see figures 2-3) of each of said module substrates (18, 28) so that the direction of arrangement of said connecting terminals (36) of an upper substrate (28) is substantially perpendicular (top view from figure 3) to the direction of arrangement of said connecting terminals (26) of a lower substrate (18).

Regarding claim 17, Fogal et al disclose a ratio of a length to a width of each of said module substrates is within a range of about 1/3 to about 1/1, see figure 1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 7 and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. (US 5,323,060) or Fogal et al. (US 5,874,781) in view of Mandai et al. (U. S. Patent 5,726,612).

Fogal et al. ('060) or Fogal et al. ('781) disclose all of the limitations of the claimed invention as explained in claim 5, except for the module substrates have a nozzle suction area that is arranged to be drawn by a component transporting suction nozzle.

Mandai teach a nozzle suction (3) formed electronic components on a substrate (1) disclosed in figure 1.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a nozzle suction in the structure of Fogal et al. as taught by Mandai in order to place components mounting on a PCB and also prevent ESD for the components when they are mounted on PCB.

10. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. (US 5,323,060) or Fogal et al. (US 5,874,781) in view of Prior Art (figure 12, admitted by applicant, hereafter APA).

Fogal et al. ('060) or ('781) disclose all the limitations of the claimed invention as detailed above, except for each of said module substrates having a converter power supply circuit.

PA (figure 12) shows a module substrate (49), which is a DC-DC converter device.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a module substrate having a converter power supply circuit in the structure of Fogal et al. as taught by Mandai in order to convert input DC voltage and current into output DC voltage and current of the module substrate mounting structure.

Allowable Subject Matter

11. Claims 1-4, and 10-14 are allowed.

The following is an examiner's statement of reasons for allowance:

The references cited in this and the previous office actions disclose a module substrate mounting structure having a motherboard and a plurality of module substrate, and some other claim elements. However, they do not disclose a plurality of rows of connecting pads of the motherboard are arranged to be sequentially offset from one another from an inner region of the motherboard where the module substrates are mounted toward an outer region of the motherboard, connecting members of an upper module substrate of the plurality of module substrates are electrically connected to an outer row of connecting pads and connecting members of a lower module substrate of the plurality of module substrates are electrically connected to an inner row of connecting pads disposed inwardly of the outer row of connecting pads.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments filed 01/09/02 have been fully considered but they are not persuasive.

Applicant argues:

(a) Fogal et al ('060) fails to teach "said connecting pads connected to said connecting terminals arranged along the edge portion of each of said plurality of module substrates via said connecting members are arranged in the same row."

(b) Fogal et al ('060) fails to teach "the feature of plurality of module substrates are sequentially offset from one another in the direction parallel to the surface of said motherboard."

Examiner disagrees.

Response to argument (a), Fogal ('060) clearly discloses connecting pads (not shown) on a motherboard (12) connected to connecting terminals (the bonding pads 26, 36), which are arranged along the edge portion of each of a plurality of module substrates (18; 28) via connecting members (44; 50) of each of the plurality of module substrates (18; 28) disclosed in figure 3. Each of a pair of connecting members (44 or 50) is respectively connected between a pair of the pads of the motherboard (12) and a pair of the connecting terminals (the bonding pads 26 or 36), so that the connecting structure between the pair of the pads, connecting members, and connecting terminals are respectively arranged in the same row.

Therefore, it is believed the rejection is proper.

Response to argument (b), Fogal et al ('060) clearly discloses the plurality of module substrates (18, 28) that are stacked on the motherboard in the direction parallel to a surface of the motherboard, see figure 1, the substrates (18, 28) having the connecting members (44, 50) are offset connected on the connecting pads of the motherboard.

Therefore, it is believed the rejection is correct.

13. Applicant's arguments with respect to claims 15-18 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments are persuasive on claim 15 of the previous Office action. However, by apply a new art, Fogal et al. ('781) discloses all of the limitations as explained in portion #7.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin and Shim et al. disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
March 18, 2004.

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SUPERVISORY PATENT EXAMINER
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